



The Delphion Integrated View

Get Now: ☒ PDF | [More choices...](#)Tools: [Annotate](#) | Add to Work File: [Create new Work File](#) View: [INPADOC](#) | Jump to: [Top](#)Go to: [Derwent...](#)☐ [Email this to a friend](#)

🔍 Title: **JP2002027464A2: ENCODER AND DECODER**

🔍 Country: **JP Japan**

🔍 Kind: **A2 Document Laid open to Public inspection**

🔍 Inventor: **SHIMODA KANEYASU;**

🔍 Assignee: **FUJITSU LTD**
[News, Profiles, Stocks and More about this company](#)

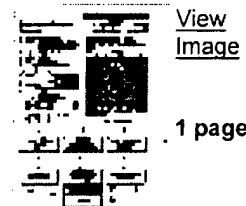
🔍 Published / Filed: **2002-01-25 / 2000-07-07**

🔍 Application Number: **JP2000000207448**

🔍 IPC Code: **H04N 7/24; G11B 20/10; G11B 20/18; H03M 7/14; H03M 13/27;**

🔍 Priority Number: **2000-07-07 JP2000000207448**

🔍 Abstract:



PROBLEM TO BE SOLVED: To provide an encoder and a decoder which improve an error propagation suppression and ECC correction ability while avoiding increase in circuit size.

SOLUTION: The encoder includes a means for branching an RLL code into a restraining part corresponding to a basic code and a non-restraining part corresponding to an information bit itself, a first encoder means for adding an error correction code to the restraining part for RLL encoding, a second encoder means for adding an error correction code to the non-restraining part, and an interleave means for interleaving outputs of the first and second encoder means to output encoded information.

COPYRIGHT: (C)2002,JPO

🔍 INPADOC Legal Status: None Get Now: [Family Legal Status Report](#)🔍 Family: [Show 2 known family members](#)🔍 Other Abstract Info: **DERABS G2002-386795**[Nominate this for the Gallery...](#)